FIG. 1

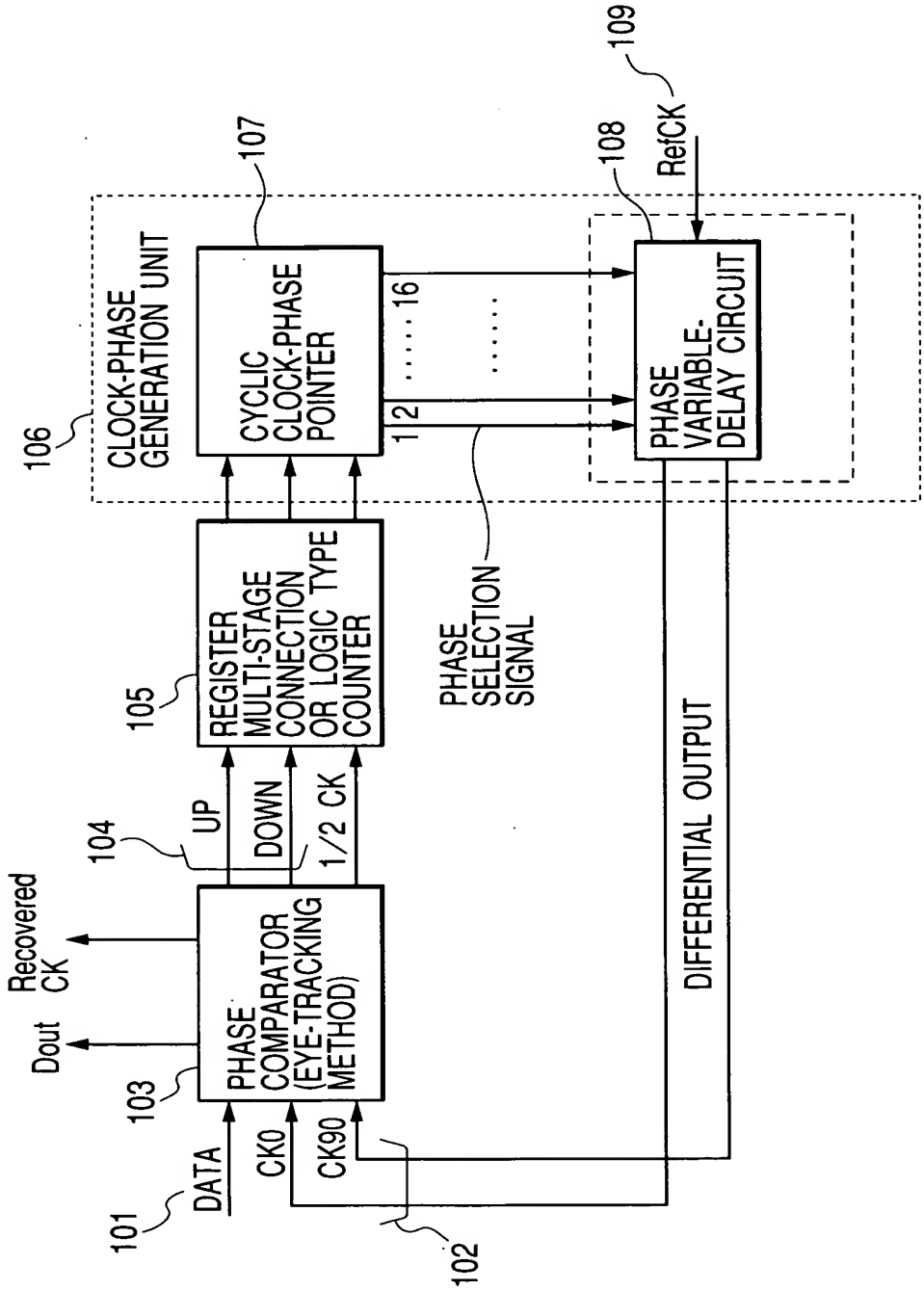

101
DATA
CK0
CK90
102
103
PHASE COMPARATOR (EYE-TRACKING METHOD)
Dout
Recovered CK
104
UP
DOWN
1/2 CK
105
REGISTER MULTI-STAGE CONNECTION OR LOGIC TYPE COUNTER
106
CLOCK-PHASE GENERATION UNIT
107
CYCLIC CLOCK-PHASE POINTER
1
2
16
PHASE SELECTION SIGNAL
108
PHASE VARIABLE-DELAY CIRCUIT
109
RefCK
DIFFERENTIAL OUTPUT

FIG. 2

CLOCK DELAY Di (UI) : DELAY TIME BETWEEN CLOCK SELECTION AND CLOCK OUTPUTTING

PHASE DETECTION PERIOD Tp (UI) : TIME IT TAKES TO PERFORM PHASE COMPARISON AND AN OR LOGIC PROCESS

CLOCK CONTROL INTERVAL Tg (UI) : CLOCK-PHASE-SWITCHING PITCH = PHASE DETECTION PERIOD Tp + CLOCK DELAY Di

LOOP DELAY (UI) : CLOCK DELAY + 1 PHASE-COMPARISON CYCLE

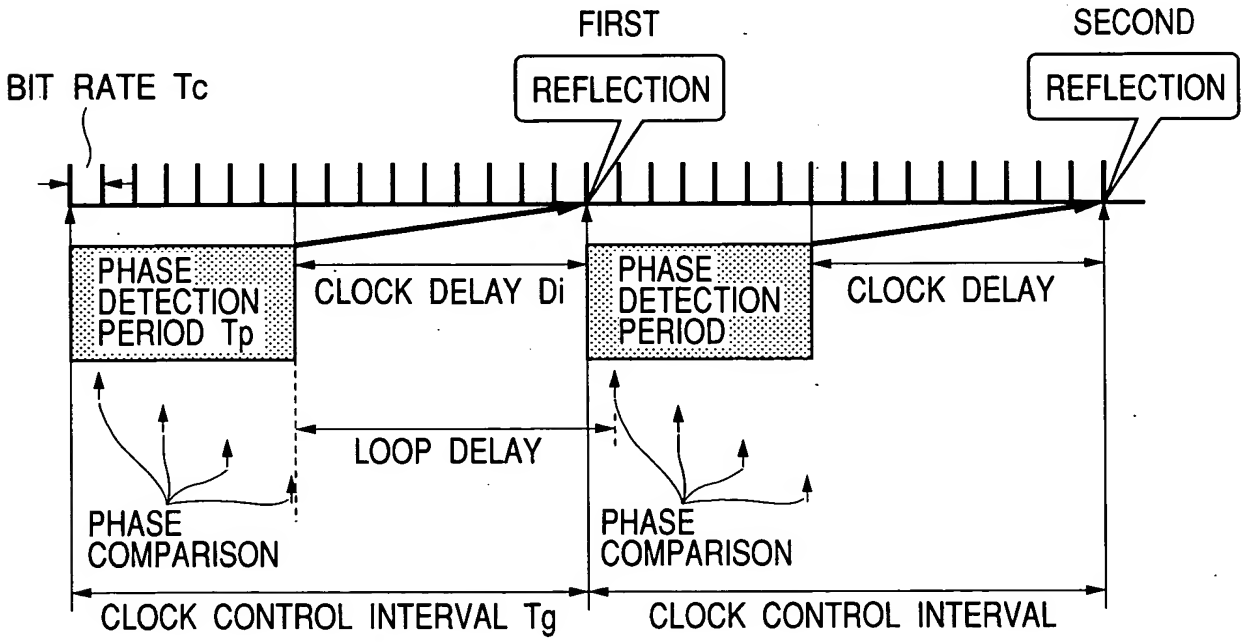


FIG. 3

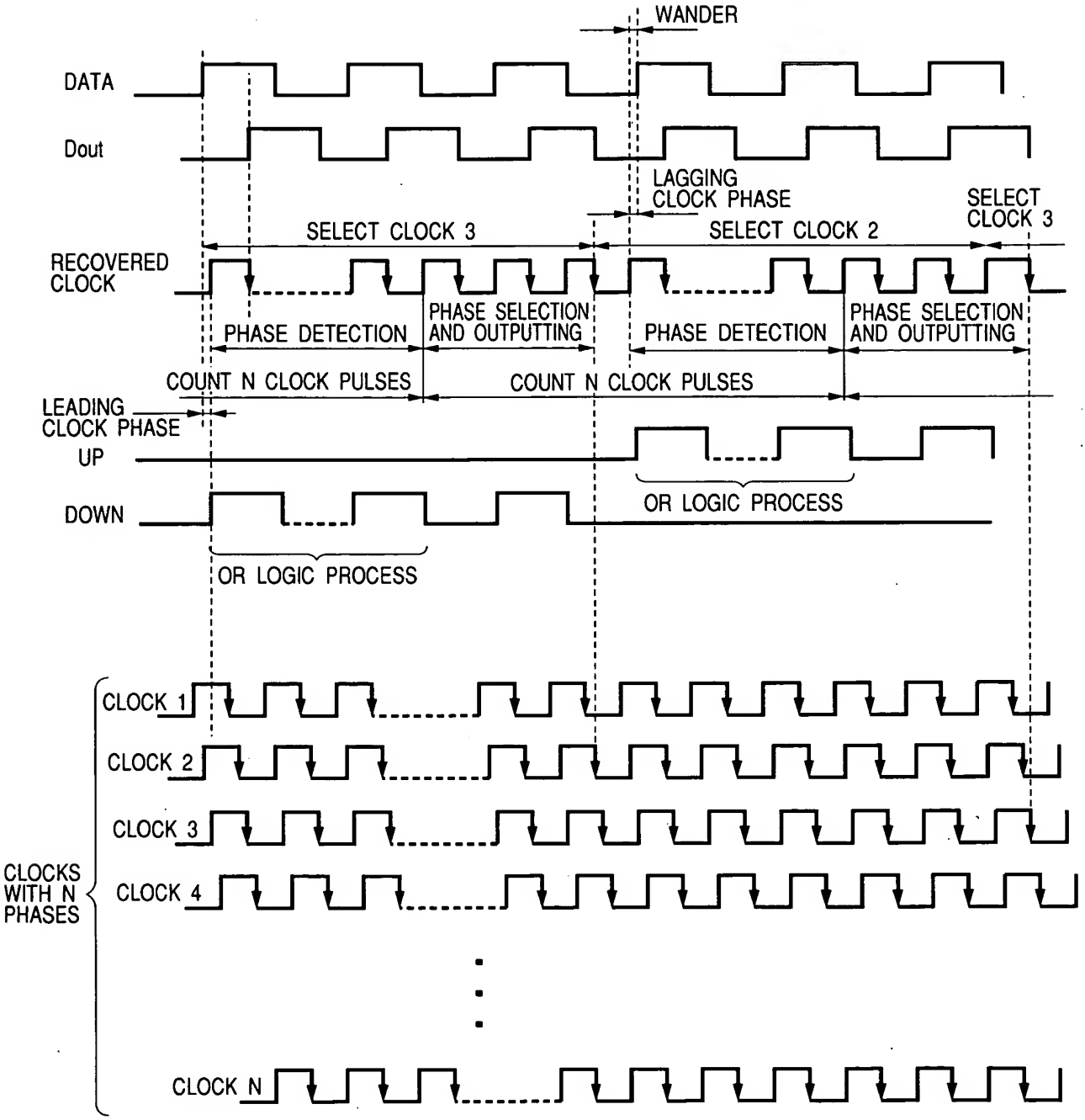

WANDER
DATA
Dout
LAGGING CLOCK PHASE
SELECT CLOCK 3
SELECT CLOCK 2
SELECT CLOCK 3
RECOVERED CLOCK
PHASE DETECTION
PHASE SELECTION AND OUTPUTTING
PHASE DETECTION
PHASE SELECTION AND OUTPUTTING
COUNT N CLOCK PULSES
COUNT N CLOCK PULSES
LEADING CLOCK PHASE
UP
OR LOGIC PROCESS
DOWN
OR LOGIC PROCESS
CLOCK 1
CLOCK 2
CLOCK 3
CLOCKS WITH N PHASES
CLOCK 4
CLOCK N

FIG. 4

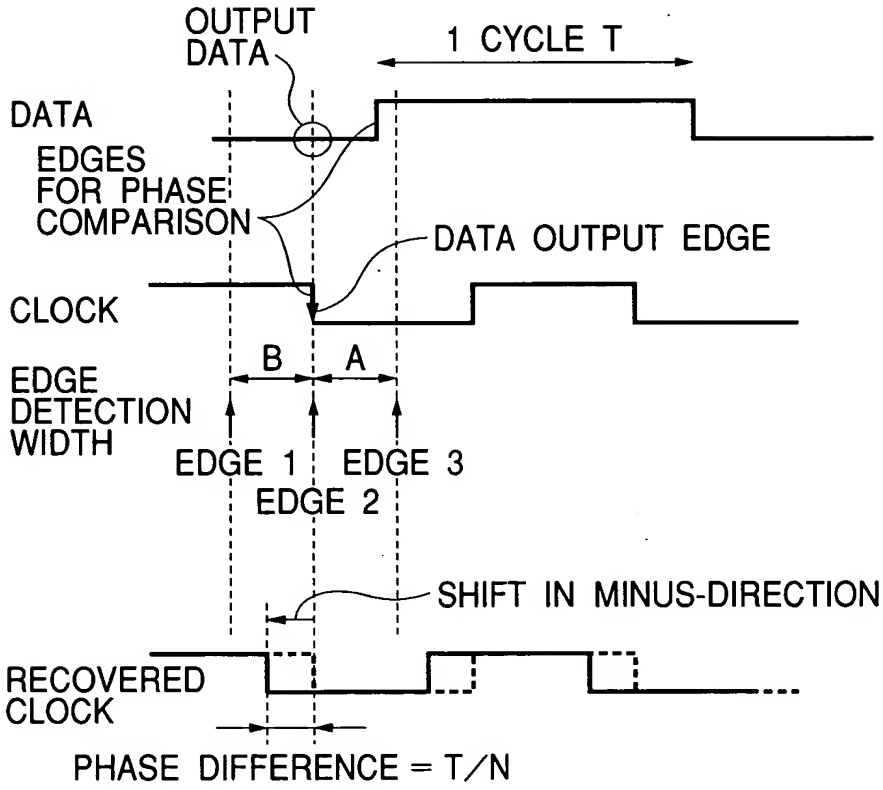

OUTPUT DATA
1 CYCLE T
DATA
EDGES FOR PHASE COMPARISON
DATA OUTPUT EDGE
CLOCK
B
A
EDGE DETECTION WIDTH
EDGE 1
EDGE 2
EDGE 3
SHIFT IN MINUS-DIRECTION
RECOVERED CLOCK
PHASE DIFFERENCE = T/N

FIG. 5

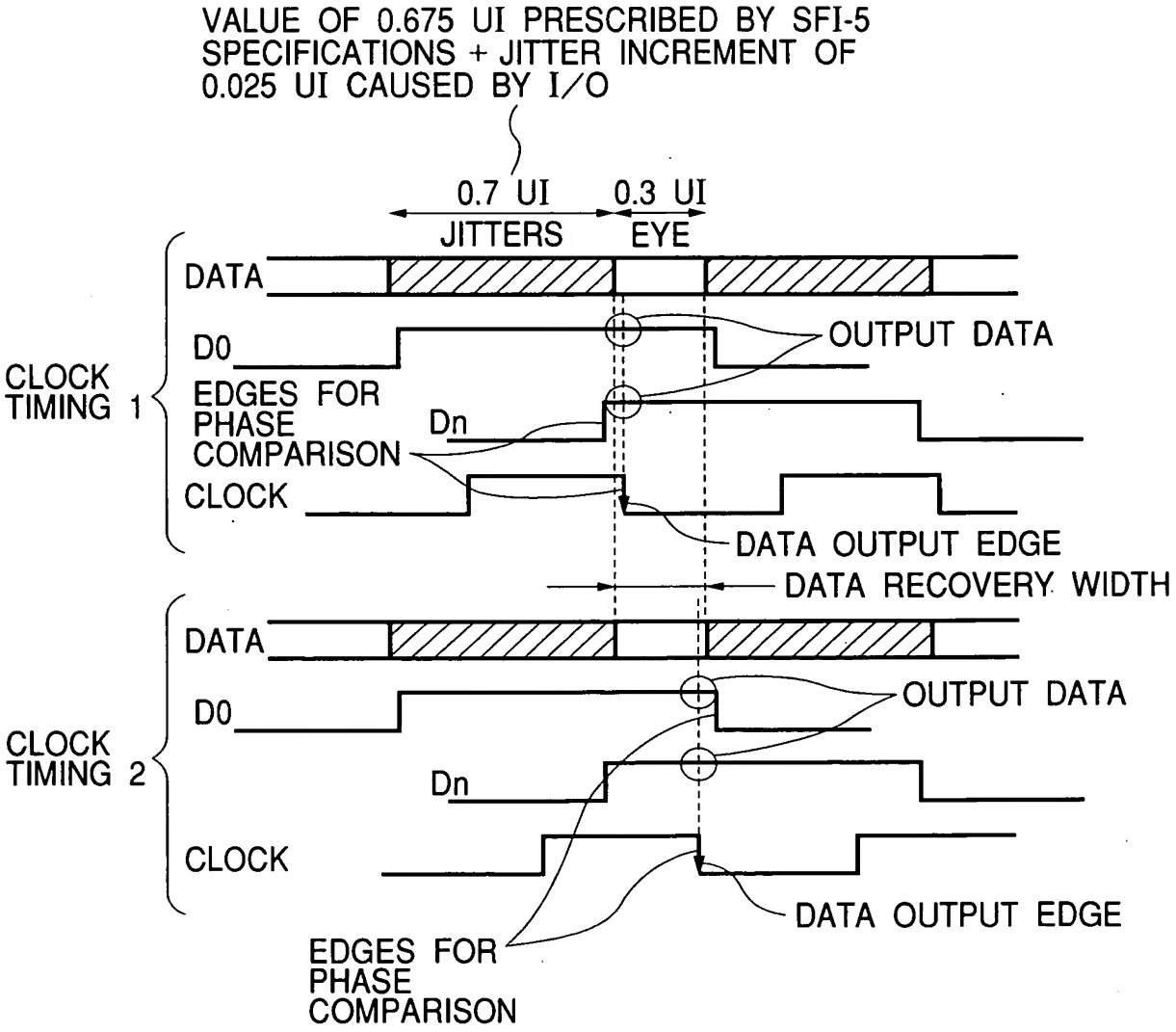

VALUE OF 0.675 UI PRESCRIBED BY SFI-5 SPECIFICATIONS + JITTER INCREMENT OF 0.025 UI CAUSED BY I/O
0.7 UI
JITTERS
0.3 UI
EYE
CLOCK TIMING 1
DATA
D0
OUTPUT DATA
EDGES FOR PHASE COMPARISON
Dn
CLOCK
DATA OUTPUT EDGE
DATA RECOVERY WIDTH
CLOCK TIMING 2
DATA
D0
OUTPUT DATA
Dn
CLOCK
DATA OUTPUT EDGE
EDGES FOR PHASE COMPARISON

FIG. 6

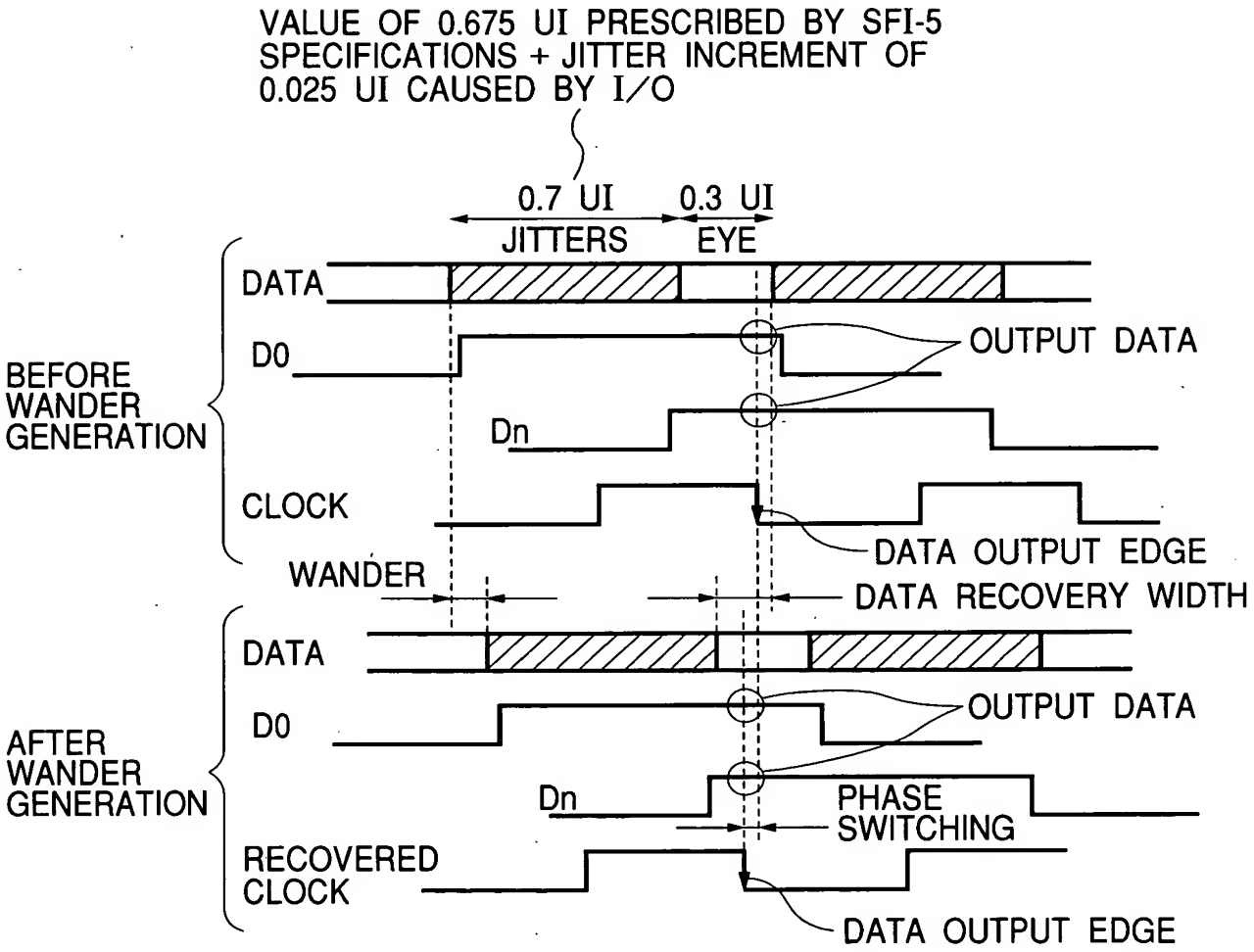

VALUE OF 0.675 UI PRESCRIBED BY SFI-5 SPECIFICATIONS + JITTER INCREMENT OF 0.025 UI CAUSED BY I/O
0.7 UI
JITTERS
0.3 UI
EYE
DATA
D0
OUTPUT DATA
Dn
BEFORE WANDER GENERATION
CLOCK
DATA OUTPUT EDGE
WANDER
DATA RECOVERY WIDTH
DATA
D0
OUTPUT DATA
AFTER WANDER GENERATION
Dn
PHASE SWITCHING
RECOVERED CLOCK
DATA OUTPUT EDGE

FIG. 7

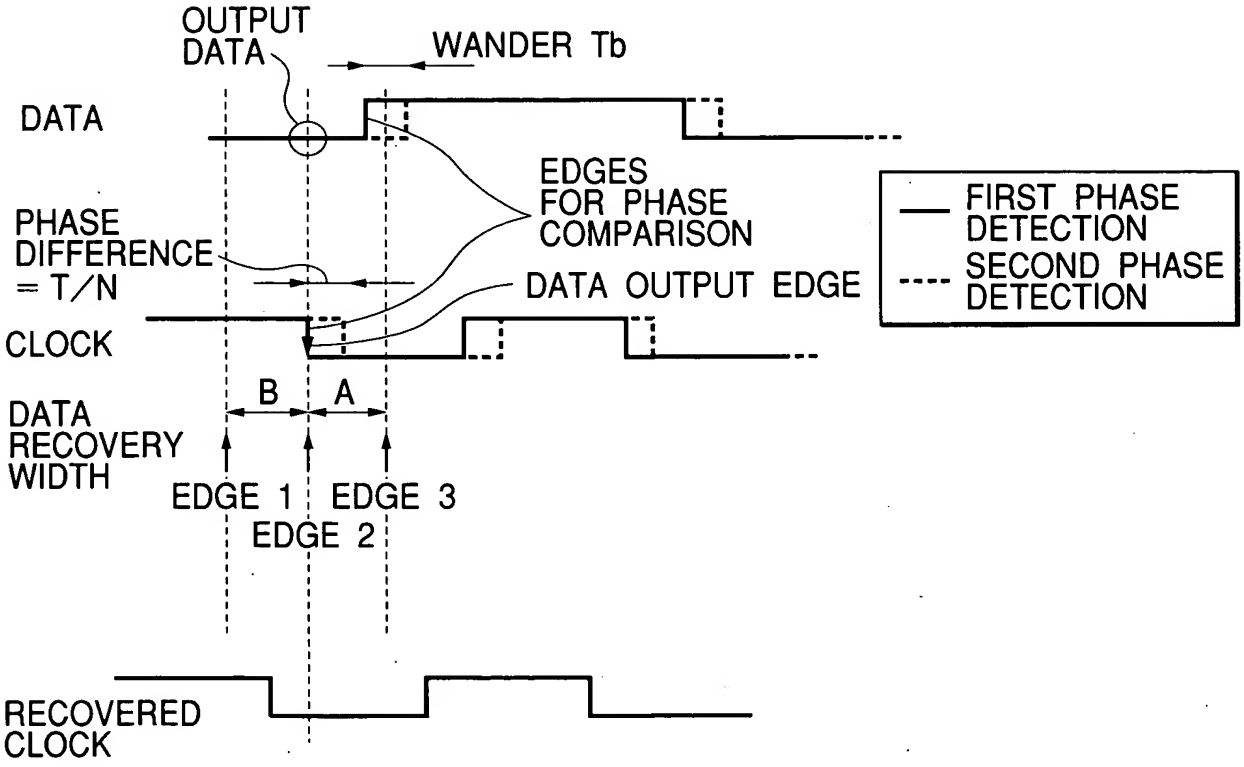

OUTPUT DATA
WANDER Tb
DATA
EDGES FOR PHASE COMPARISON
PHASE DIFFERENCE = T/N
DATA OUTPUT EDGE
CLOCK
B
A
DATA RECOVERY WIDTH
EDGE 1
EDGE 3
EDGE 2
RECOVERED CLOCK
FIRST PHASE DETECTION
SECOND PHASE DETECTION

FIG. 8

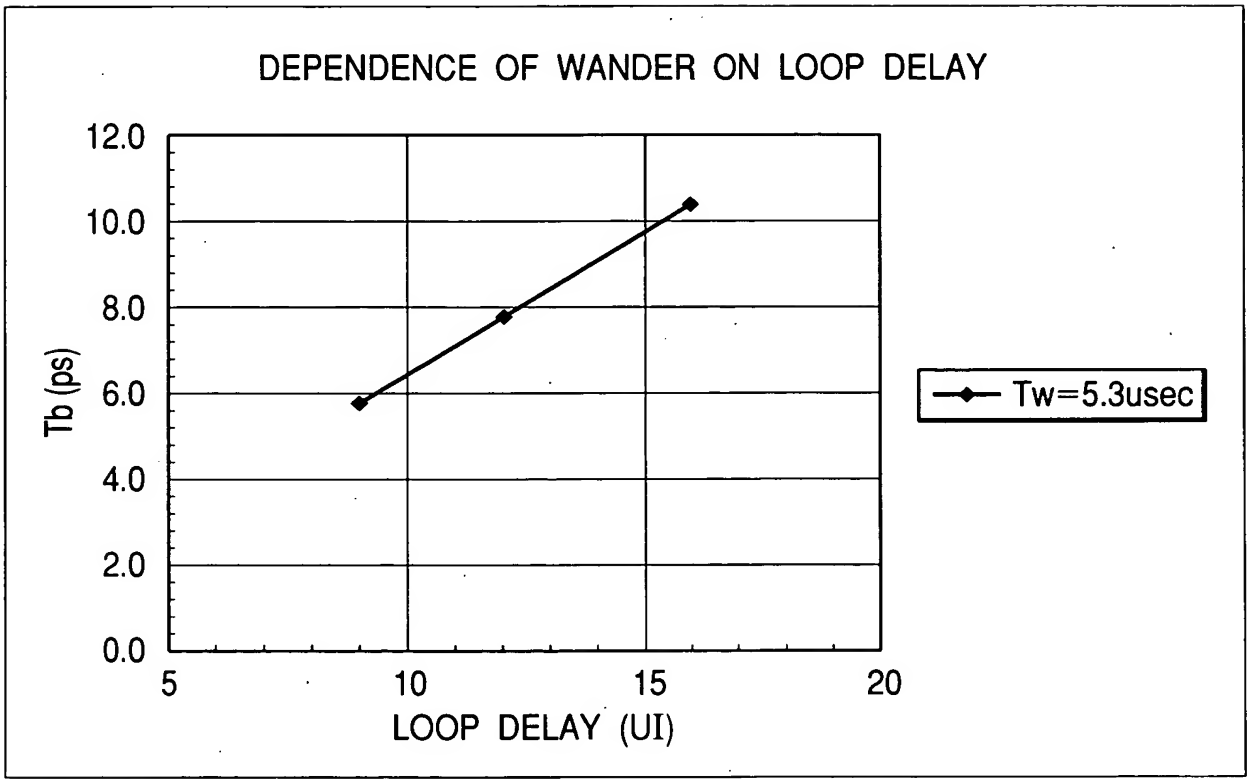

DEPENDENCE OF WANDER ON LOOP DELAY
12.0
10.0
8.0
6.0
4.0
2.0
0.0
Tb (ps)
5
10
15
20
LOOP DELAY (UI)
Tw=5.3usec

FIG. 9

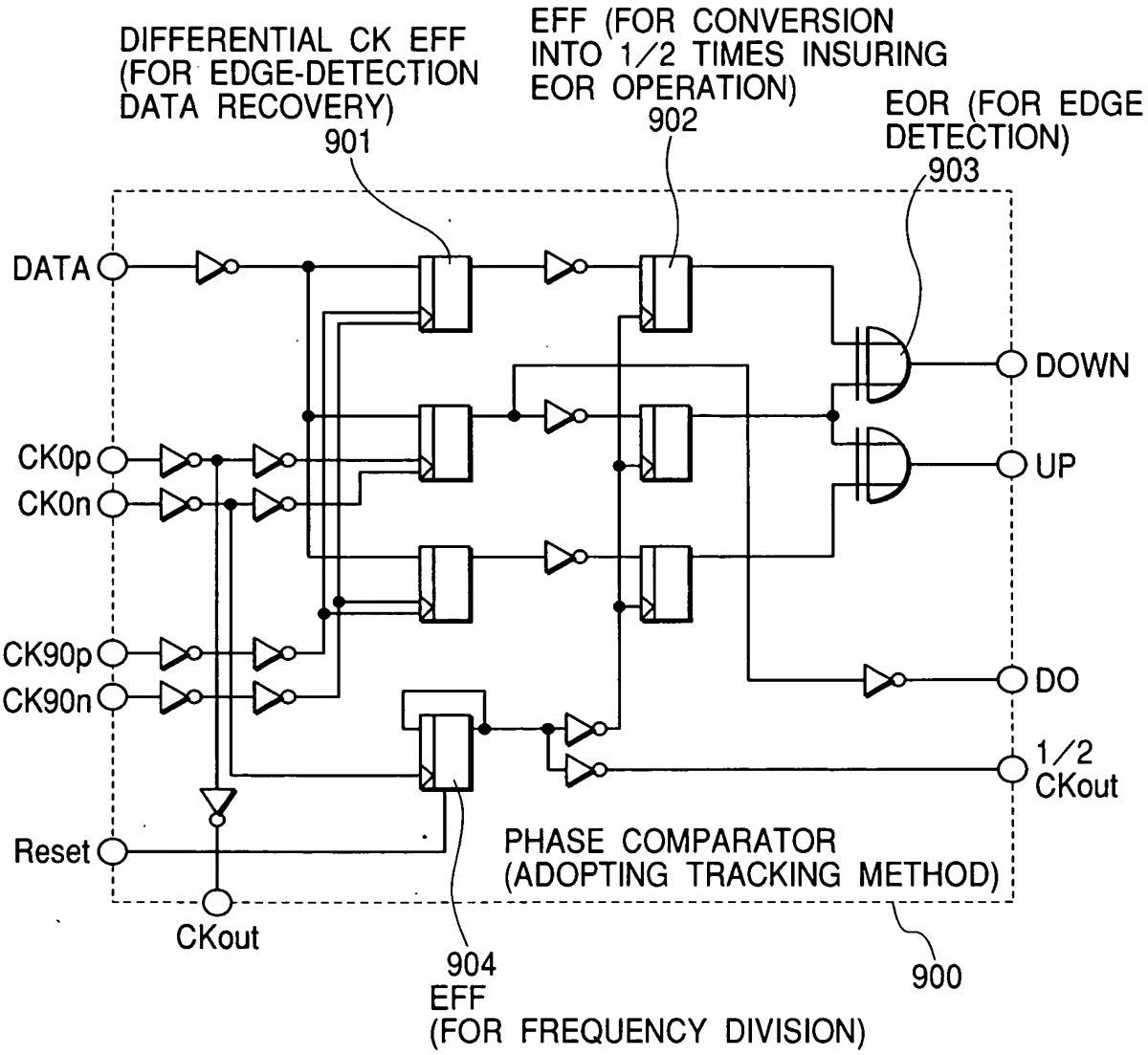

DIFFERENTIAL CK EFF
(FOR EDGE-DETECTION
DATA RECOVERY)
901
EFF (FOR CONVERSION
INTO 1/2 TIMES INSURING
EOR OPERATION)
902
EOR (FOR EDGE
DETECTION)
903
DATA
CK0p
CK0n
CK90p
CK90n
Reset
CKout
DOWN
UP
DO
1/2
CKout
PHASE COMPARATOR
(ADOPTING TRACKING METHOD)
900
904
EFF
(FOR FREQUENCY DIVISION)

FIG. 10

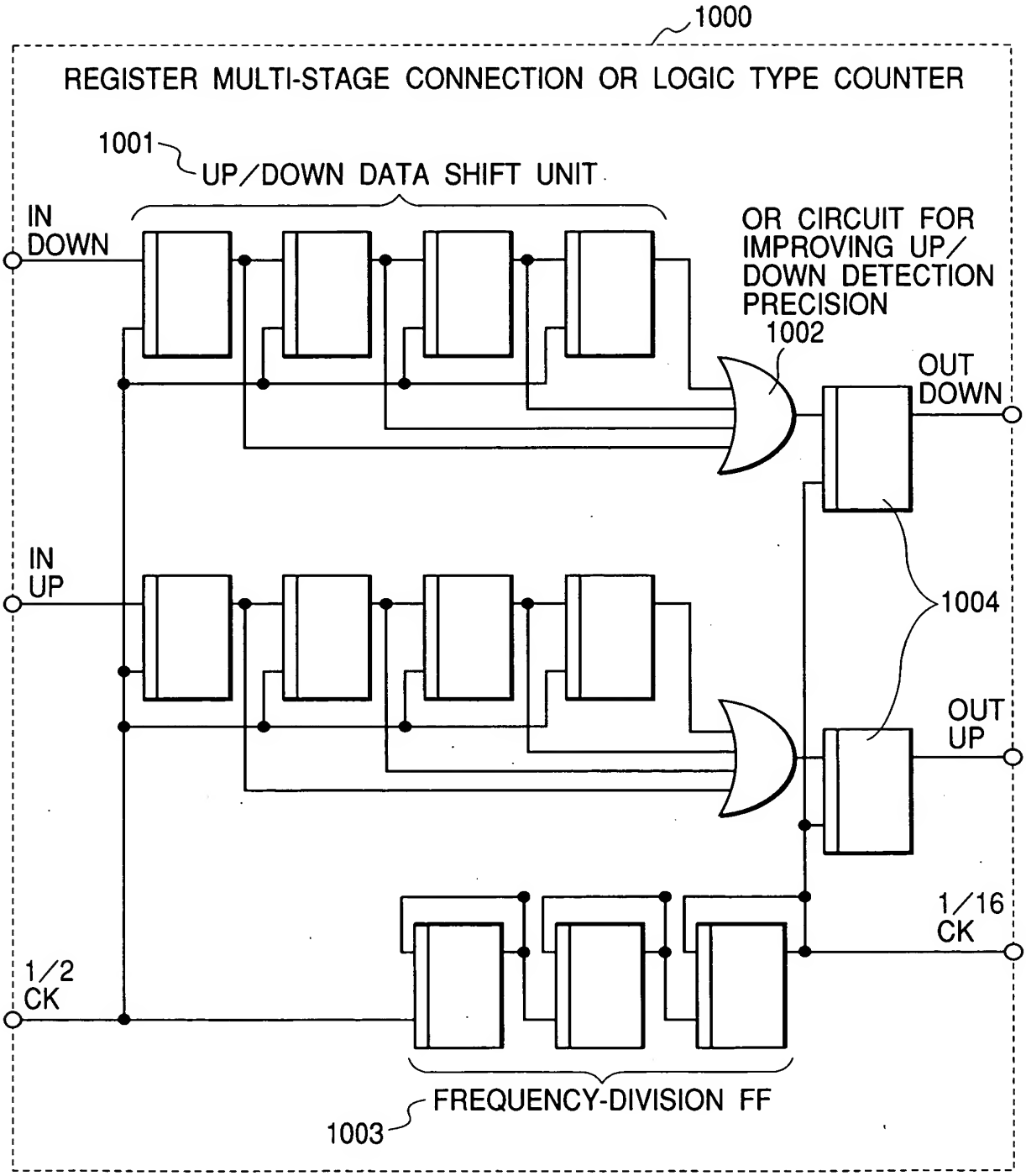

1000
REGISTER MULTI-STAGE CONNECTION OR LOGIC TYPE COUNTER
1001
UP/DOWN DATA SHIFT UNIT
IN
DOWN
OR CIRCUIT FOR IMPROVING UP/DOWN DETECTION PRECISION
1002
OUT
DOWN
IN
UP
1004
OUT
UP
1/16
CK
1/2
CK
FREQUENCY-DIVISION FF
1003

FIG. 11

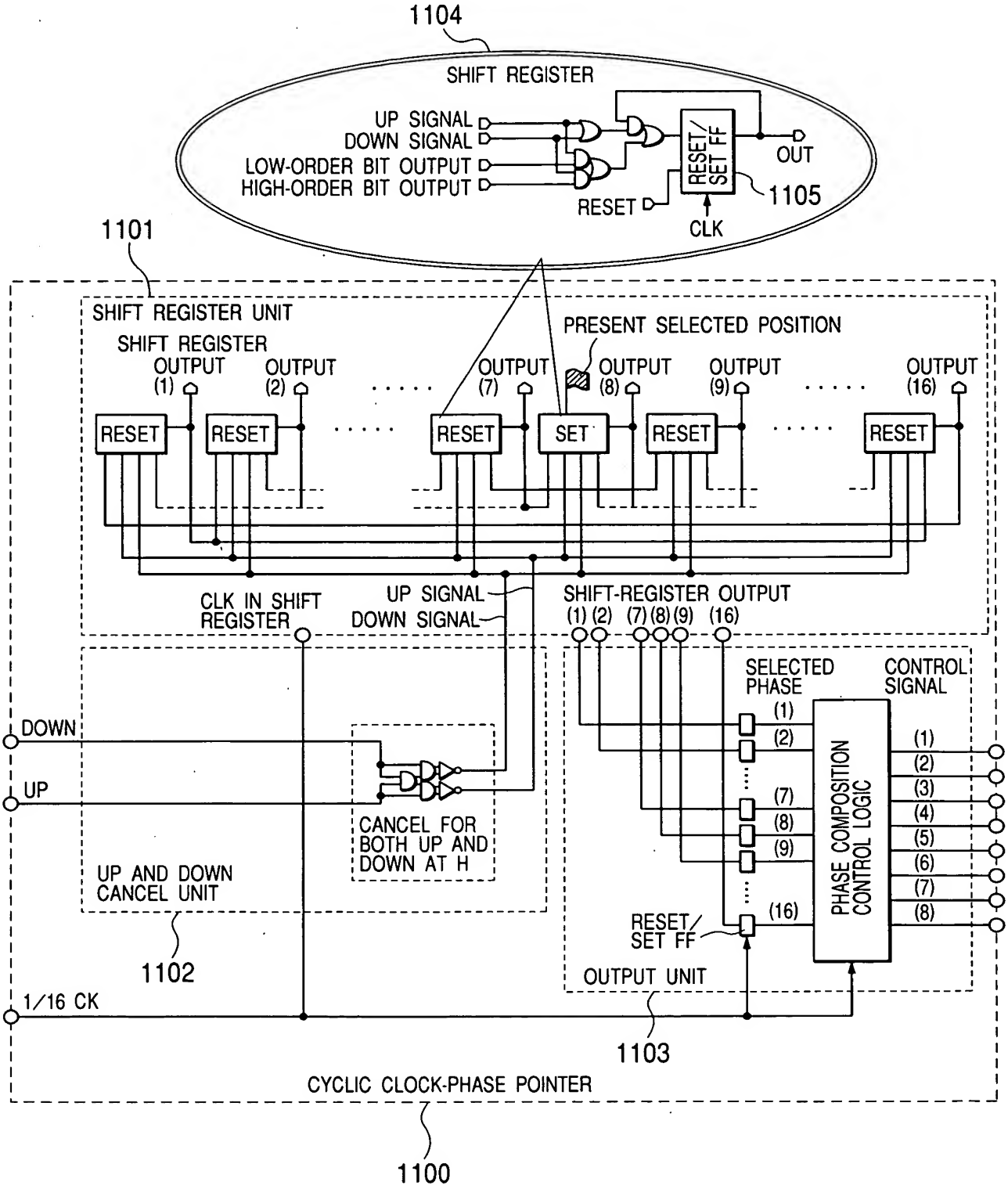

1104
SHIFT REGISTER
UP SIGNAL
DOWN SIGNAL
LOW-ORDER BIT OUTPUT
HIGH-ORDER BIT OUTPUT
RESET/ SET FF
OUT
RESET
CLK
1105
1101
SHIFT REGISTER UNIT
SHIFT REGISTER
PRESENT SELECTED POSITION
OUTPUT (1)
OUTPUT (2)
OUTPUT (7)
OUTPUT (8)
OUTPUT (9)
OUTPUT (16)
RESET
SET
CLK IN SHIFT REGISTER
UP SIGNAL
DOWN SIGNAL
SHIFT-REGISTER OUTPUT (1) (2) (7) (8) (9) (16)
SELECTED PHASE
CONTROL SIGNAL
DOWN
UP
CANCEL FOR BOTH UP AND DOWN AT H
PHASE COMPOSITION CONTROL LOGIC
UP AND DOWN CANCEL UNIT
1102
RESET/ SET FF
OUTPUT UNIT
1/16 CK
1103
CYCLIC CLOCK-PHASE POINTER
1100

FIG. 12

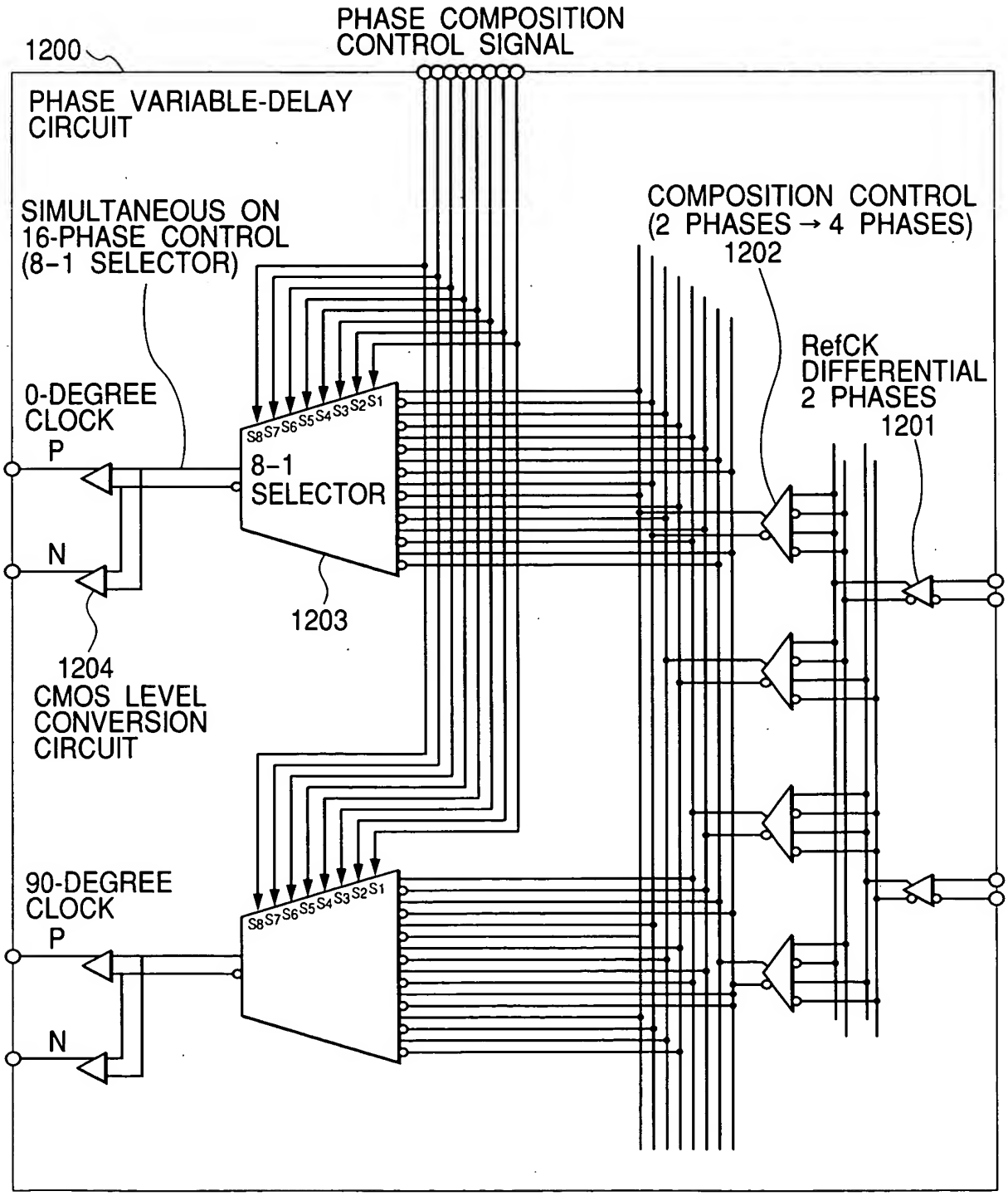

PHASE COMPOSITION
CONTROL SIGNAL
1200
PHASE VARIABLE-DELAY
CIRCUIT
SIMULTANEOUS ON
16-PHASE CONTROL
(8-1 SELECTOR)
COMPOSITION CONTROL
(2 PHASES → 4 PHASES)
1202
RefCK
DIFFERENTIAL
2 PHASES
1201
0-DEGREE
CLOCK
P
N
S8 S7 S6 S5 S4 S3 S2 S1
8-1
SELECTOR
1203
1204
CMOS LEVEL
CONVERSION
CIRCUIT
90-DEGREE
CLOCK
P
N
S8 S7 S6 S5 S4 S3 S2 S1

FIG. 13

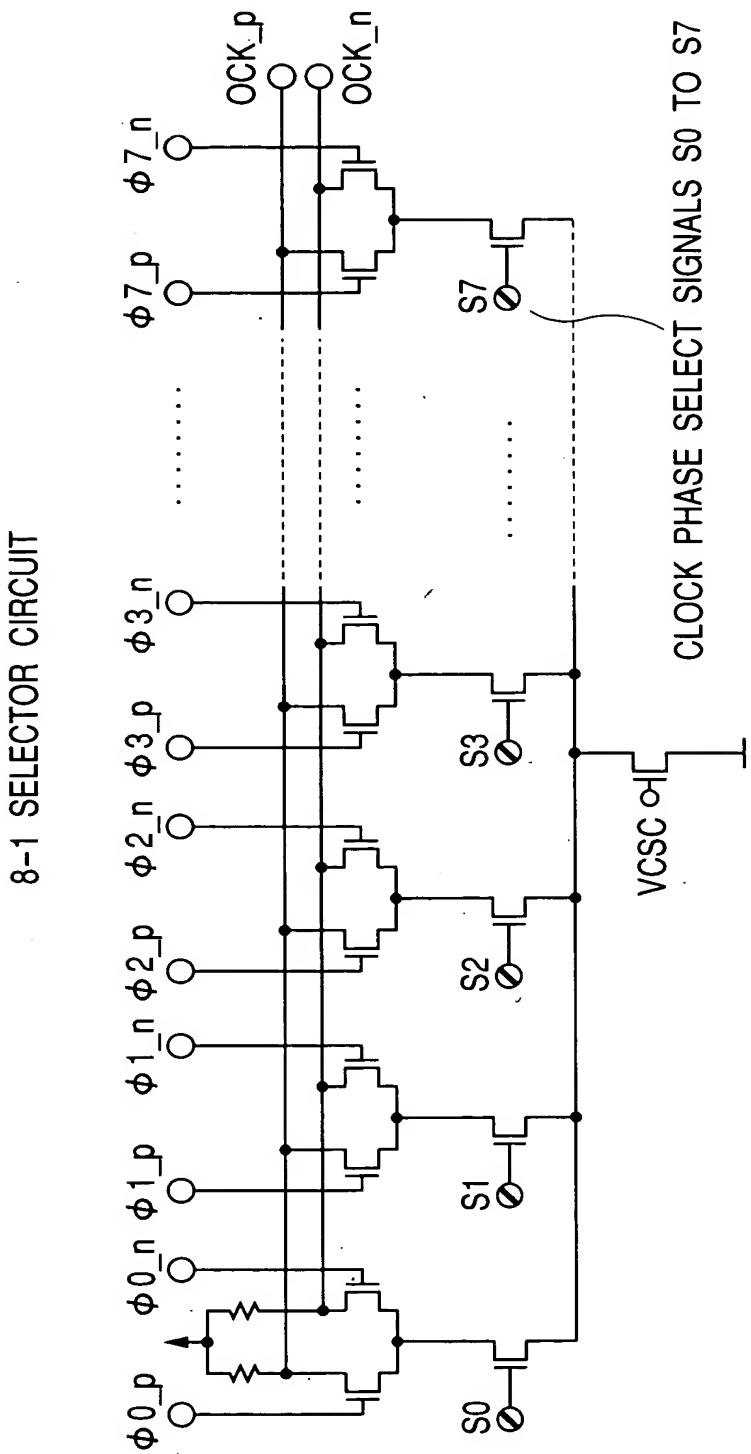

8-1 SELECTOR CIRCUIT
OCK_p
OCK_n
φ7_n
φ7_p
φ3_n
φ3_p
φ2_n
φ2_p
φ1_n
φ1_p
φ0_n
φ0_p
S7
S3
S2
S1
S0
VCSC
CLOCK PHASE SELECT SIGNALS S0 TO S7
○: DIFFERENTIAL SMALL AMPLITUDE (1.3v/1.8v)
⊘: CMOS LEVEL (0v/1.8v)

FIG. 14

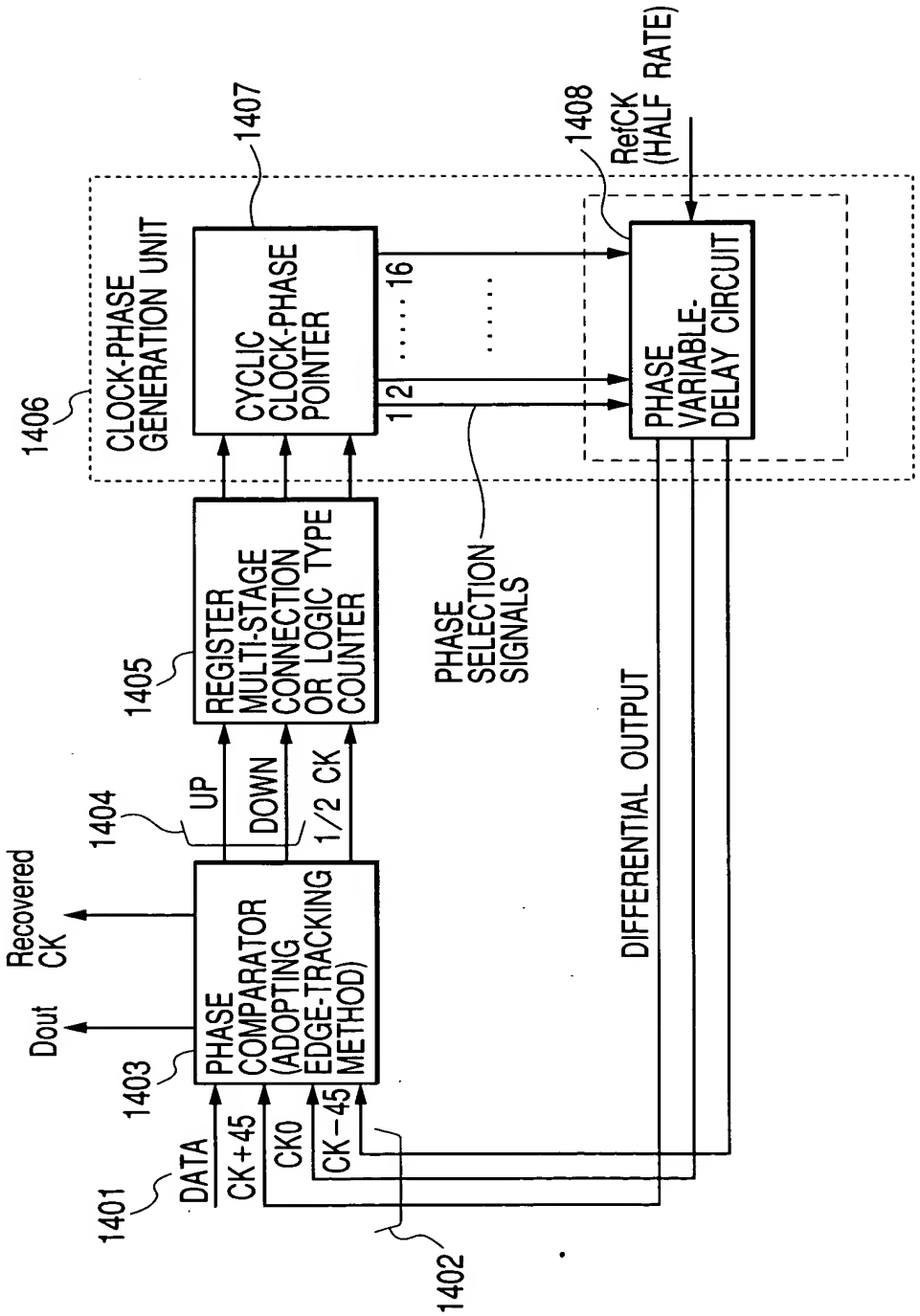

1401
DATA
CK+45
CK0
CK−45
1402
1403
PHASE COMPARATOR (ADOPTING EDGE-TRACKING METHOD)
Dout
Recovered CK
1404
UP
DOWN
1/2 CK
1405
REGISTER MULTI-STAGE CONNECTION OR LOGIC TYPE COUNTER
1406
CLOCK-PHASE GENERATION UNIT
1407
CYCLIC CLOCK-PHASE POINTER
1 2 16
PHASE SELECTION SIGNALS
1408
RefCK (HALF RATE)
PHASE VARIABLE-DELAY CIRCUIT
DIFFERENTIAL OUTPUT

FIG. 15

CONFIGURATION OF CLOCK DATA RECOVERY CIRCUIT ADOPTING DATA DELAY METHOD IN ACCORDANCE WITH FOURTH EMBODIMENT

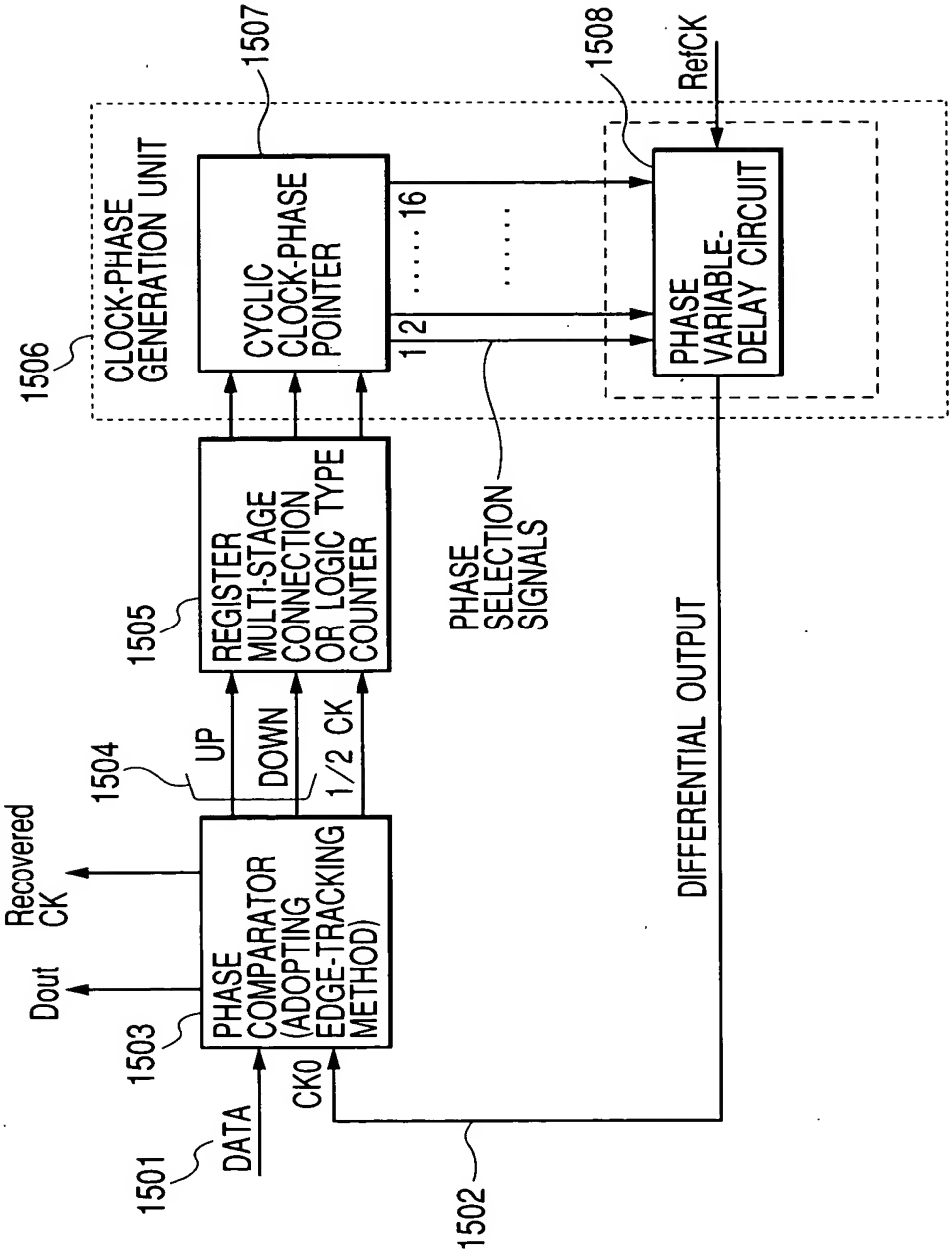


FIG. 16

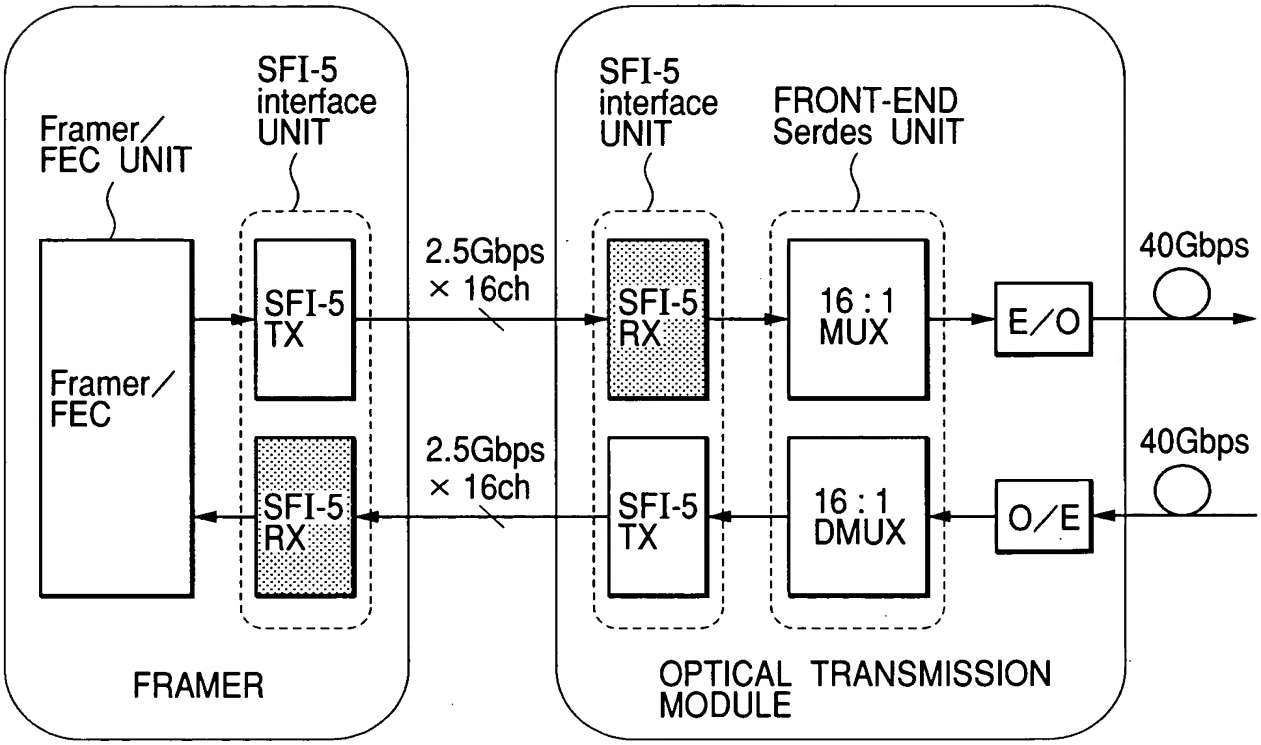

Framer/
FEC UNIT
SFI-5
interface
UNIT
Framer/
FEC
SFI-5
TX
SFI-5
RX
FRAMER
2.5Gbps
× 16ch
2.5Gbps
× 16ch
SFI-5
interface
UNIT
FRONT-END
Serdes UNIT
SFI-5
RX
SFI-5
TX
16 : 1
MUX
16 : 1
DMUX
E/O
O/E
40Gbps
40Gbps
OPTICAL TRANSMISSION
MODULE

FIG. 17

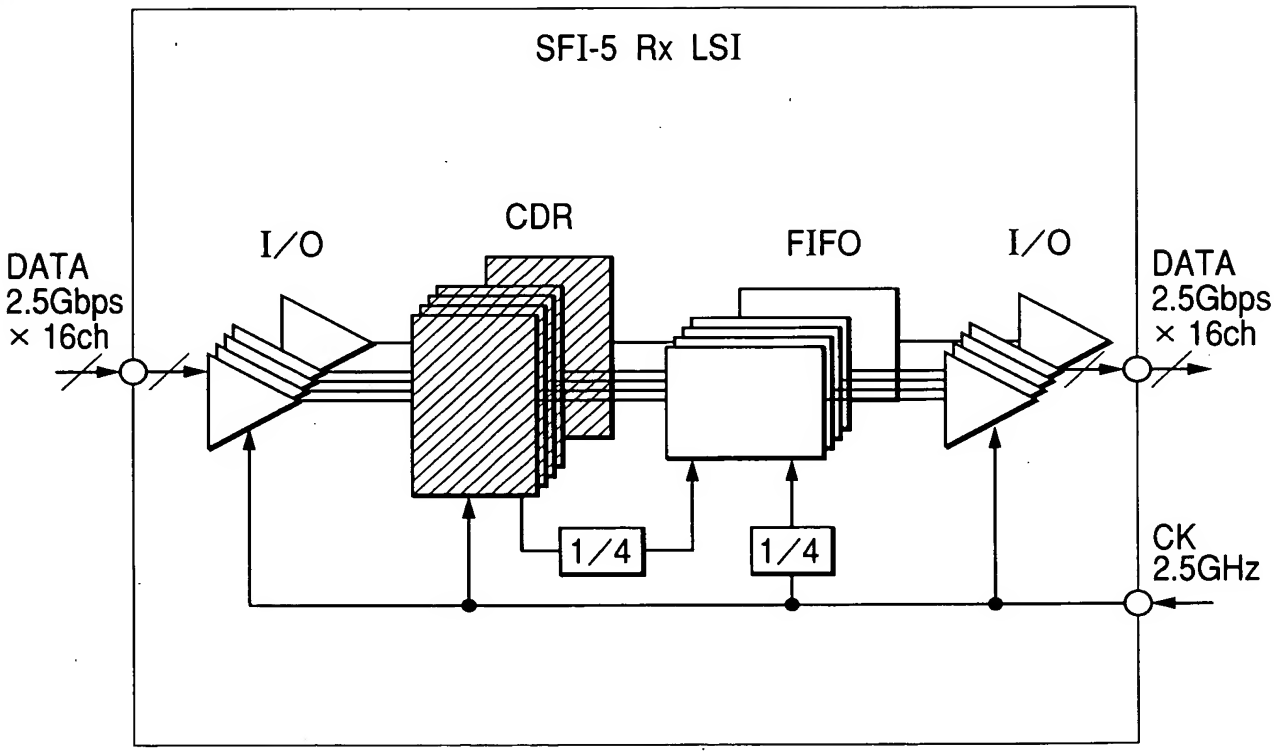

SFI-5 Rx LSI
DATA
2.5Gbps
× 16ch
I/O
CDR
FIFO
I/O
DATA
2.5Gbps
× 16ch
1/4
1/4
CK
2.5GHz

FIG. 18

BLOCK DIAGRAM OF COMPARATIVE EXAMPLE OF VCO TYPE

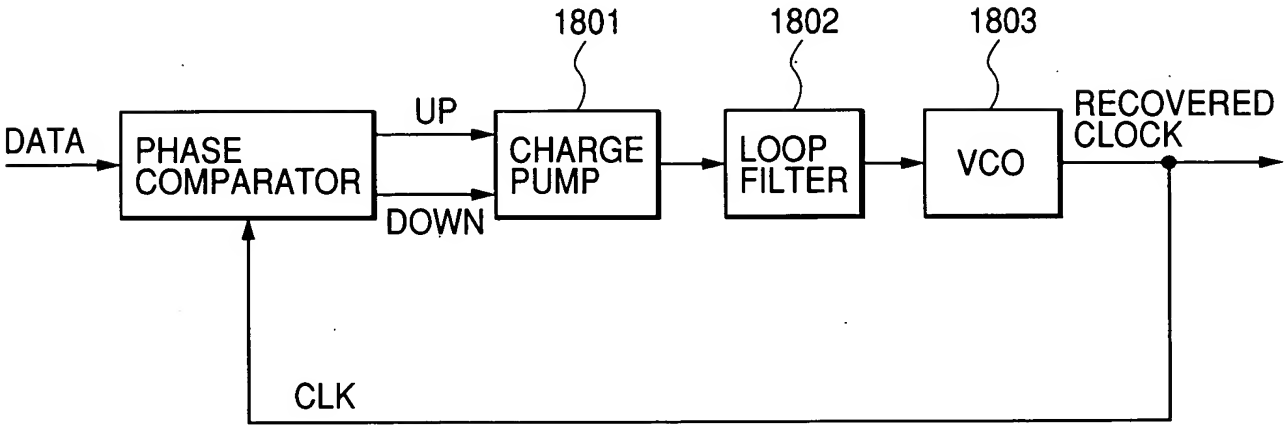


FIG. 19

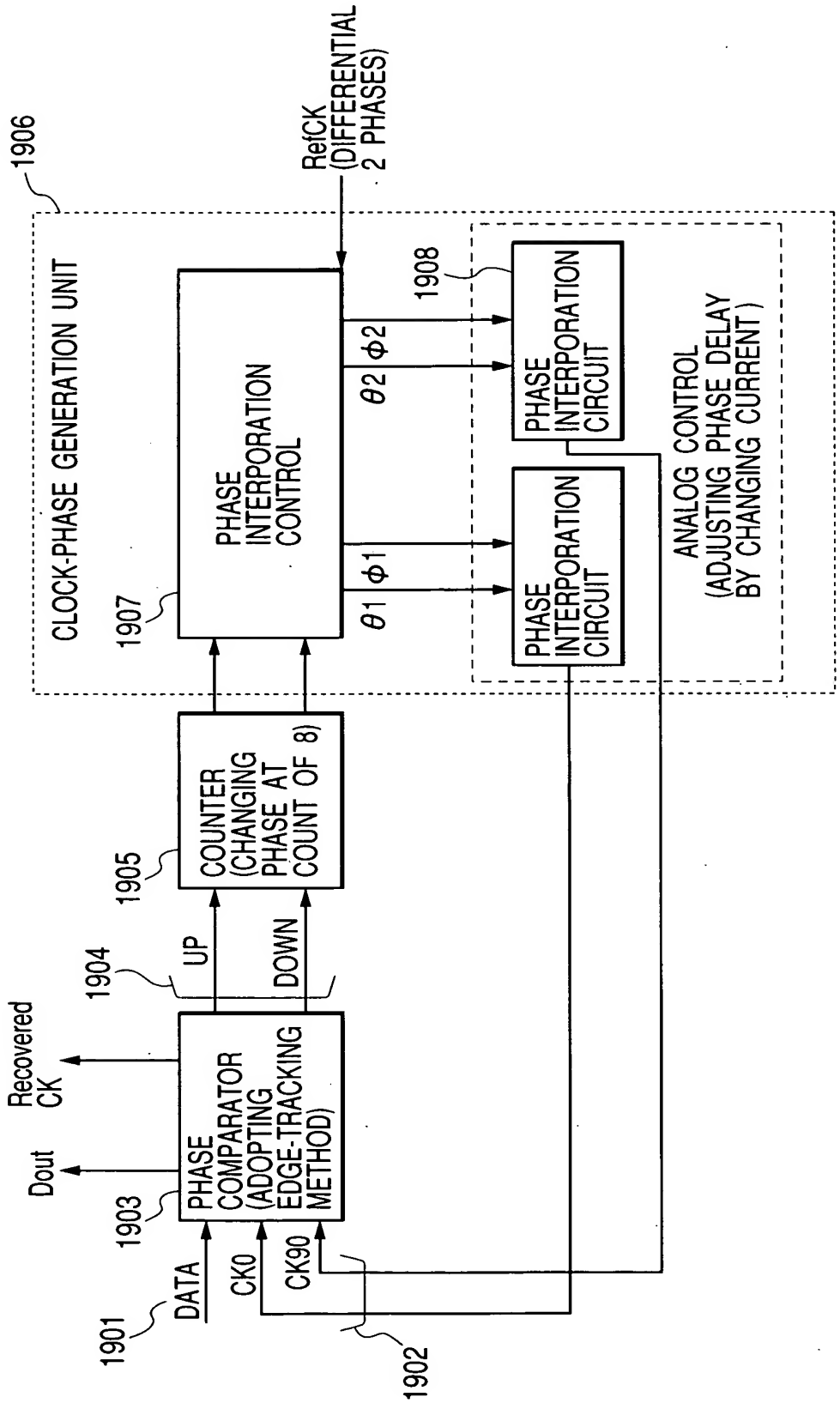

1906
CLOCK-PHASE GENERATION UNIT
RefCK (DIFFERENTIAL 2 PHASES)
1907
PHASE INTERPORATION CONTROL
θ2
φ2
θ1
φ1
1908
PHASE INTERPORATION CIRCUIT
PHASE INTERPORATION CIRCUIT
ANALOG CONTROL (ADJUSTING PHASE DELAY BY CHANGING CURRENT)
1905
COUNTER (CHANGING PHASE AT COUNT OF 8)
1904
UP
DOWN
Recovered CK
Dout
1903
PHASE COMPARATOR (ADOPTING EDGE-TRACKING METHOD)
1901
DATA
CK0
CK90
1902

FIG. 20

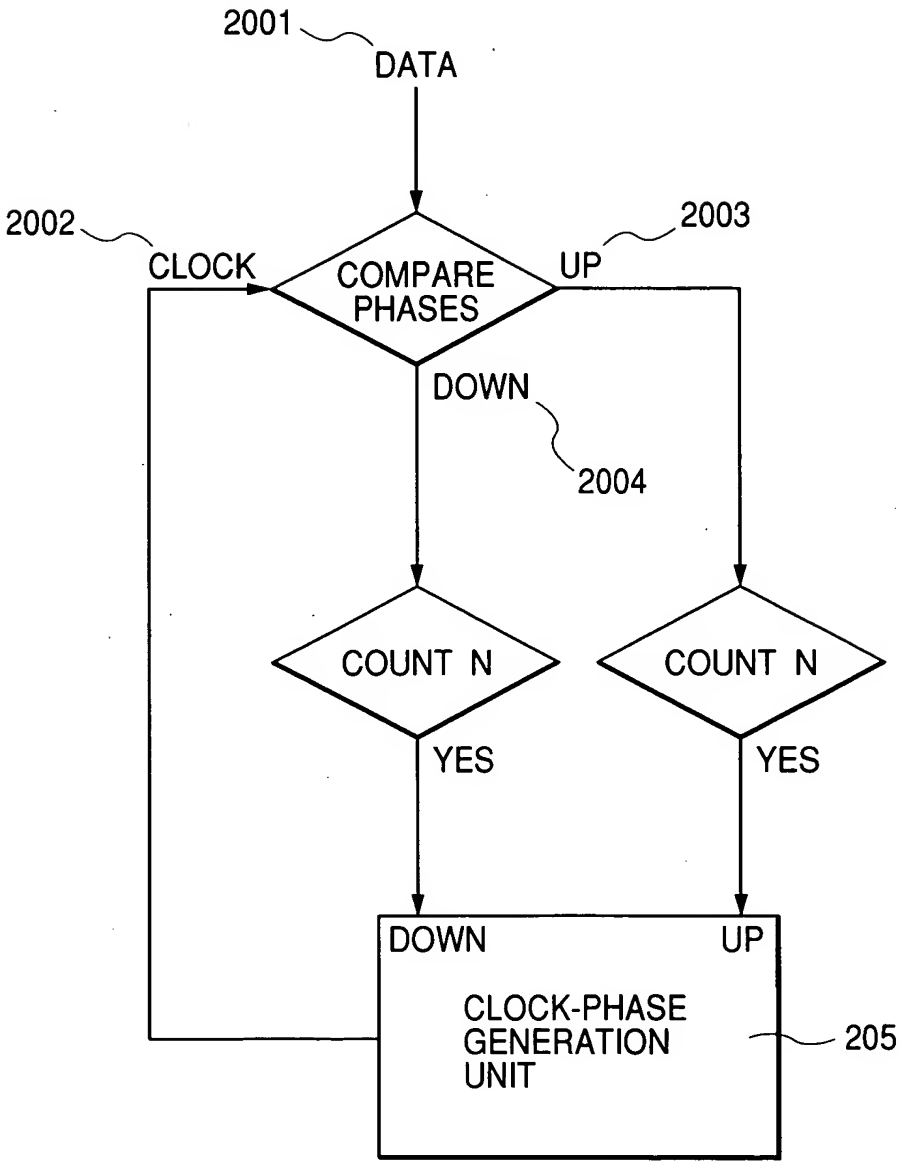

2001
DATA
2002
CLOCK
COMPARE PHASES
UP
2003
DOWN
2004
COUNT N
COUNT N
YES
YES
DOWN
UP
CLOCK-PHASE GENERATION UNIT
205

FIG. 21

CLOCK DELAY Di (UI) : DELAY TIME BETWEEN CLOCK SELECTION AND CLOCK OUTPUTTING

PHASE DETECTION PERIOD Tp (UI) : TIME IT TAKES TO PERFORM PHASE COMPARISON AND UP/DOWN COUNTING

CLOCK CONTROL INTERVAL Tg (UI) : CLOCK-PHASE-SWITCHING PITCH = PHASE DETECTION PERIOD Tp + CLOCK DELAY Di

LOOP DELAY (UI) : CLOCK DELAY + 1 PHASE-COMPARISON CYCLE

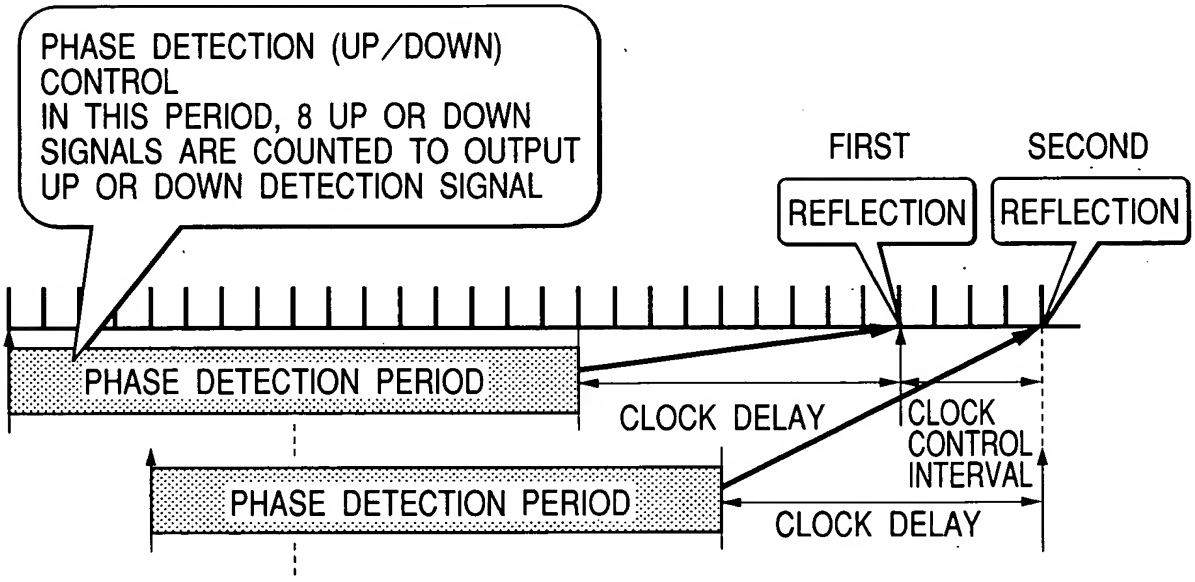


FIG. 22

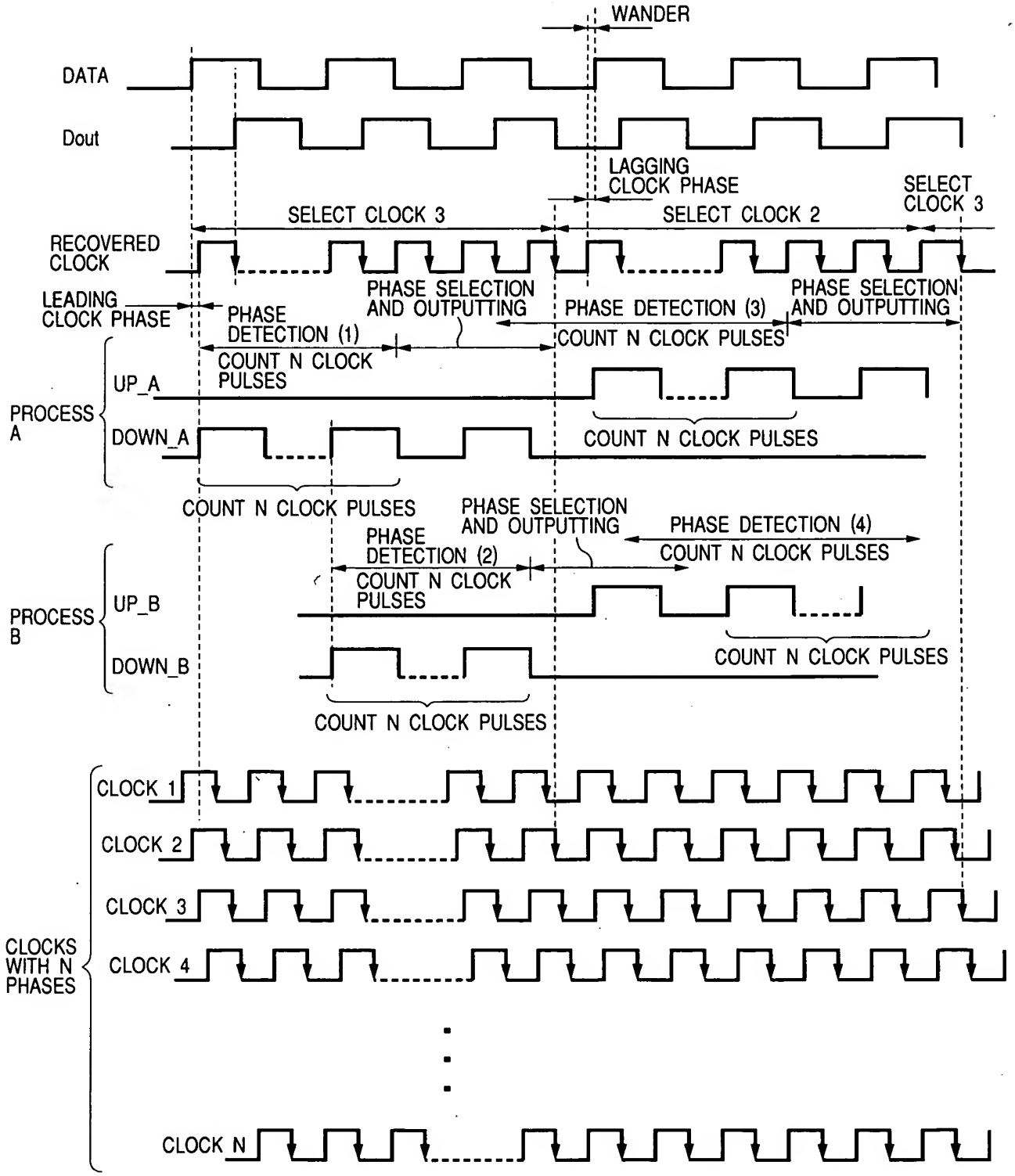

WANDER
DATA
Dout
LAGGING CLOCK PHASE
SELECT CLOCK 3
SELECT CLOCK 2
SELECT CLOCK 3
RECOVERED CLOCK
LEADING CLOCK PHASE
PHASE DETECTION (1)
PHASE SELECTION AND OUTPUTTING
PHASE DETECTION (3)
PHASE SELECTION AND OUTPUTTING
COUNT N CLOCK PULSES
COUNT N CLOCK PULSES
PROCESS A
UP_A
DOWN_A
COUNT N CLOCK PULSES
COUNT N CLOCK PULSES
PHASE SELECTION AND OUTPUTTING
PHASE DETECTION (4)
PHASE DETECTION (2)
COUNT N CLOCK PULSES
COUNT N CLOCK PULSES
PROCESS B
UP_B
DOWN_B
COUNT N CLOCK PULSES
CLOCK 1
CLOCK 2
CLOCK 3
CLOCKS WITH N PHASES
CLOCK 4
CLOCK N

FIG. 23

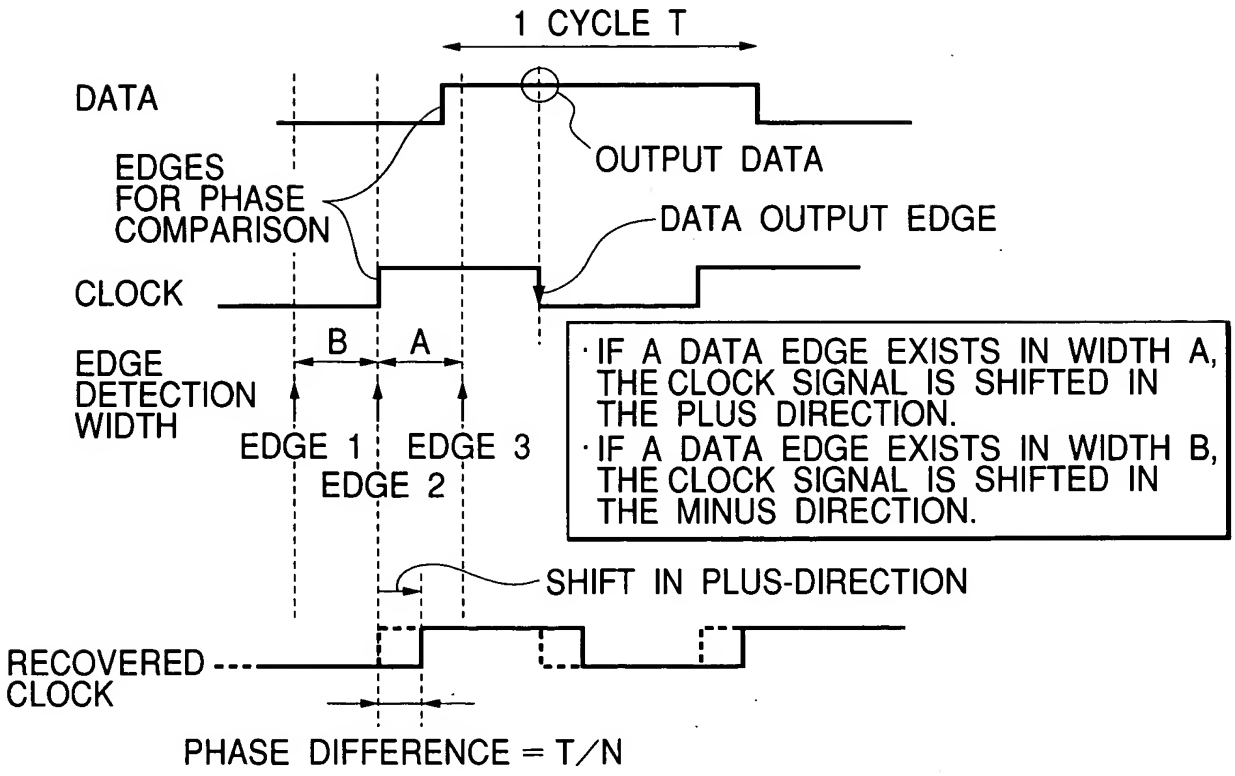

1 CYCLE T
DATA
OUTPUT DATA
EDGES FOR PHASE COMPARISON
DATA OUTPUT EDGE
CLOCK
B
A
EDGE DETECTION WIDTH
EDGE 1
EDGE 2
EDGE 3
· IF A DATA EDGE EXISTS IN WIDTH A, THE CLOCK SIGNAL IS SHIFTED IN THE PLUS DIRECTION.
· IF A DATA EDGE EXISTS IN WIDTH B, THE CLOCK SIGNAL IS SHIFTED IN THE MINUS DIRECTION.
SHIFT IN PLUS-DIRECTION
RECOVERED CLOCK
PHASE DIFFERENCE = T/N

FIG. 24

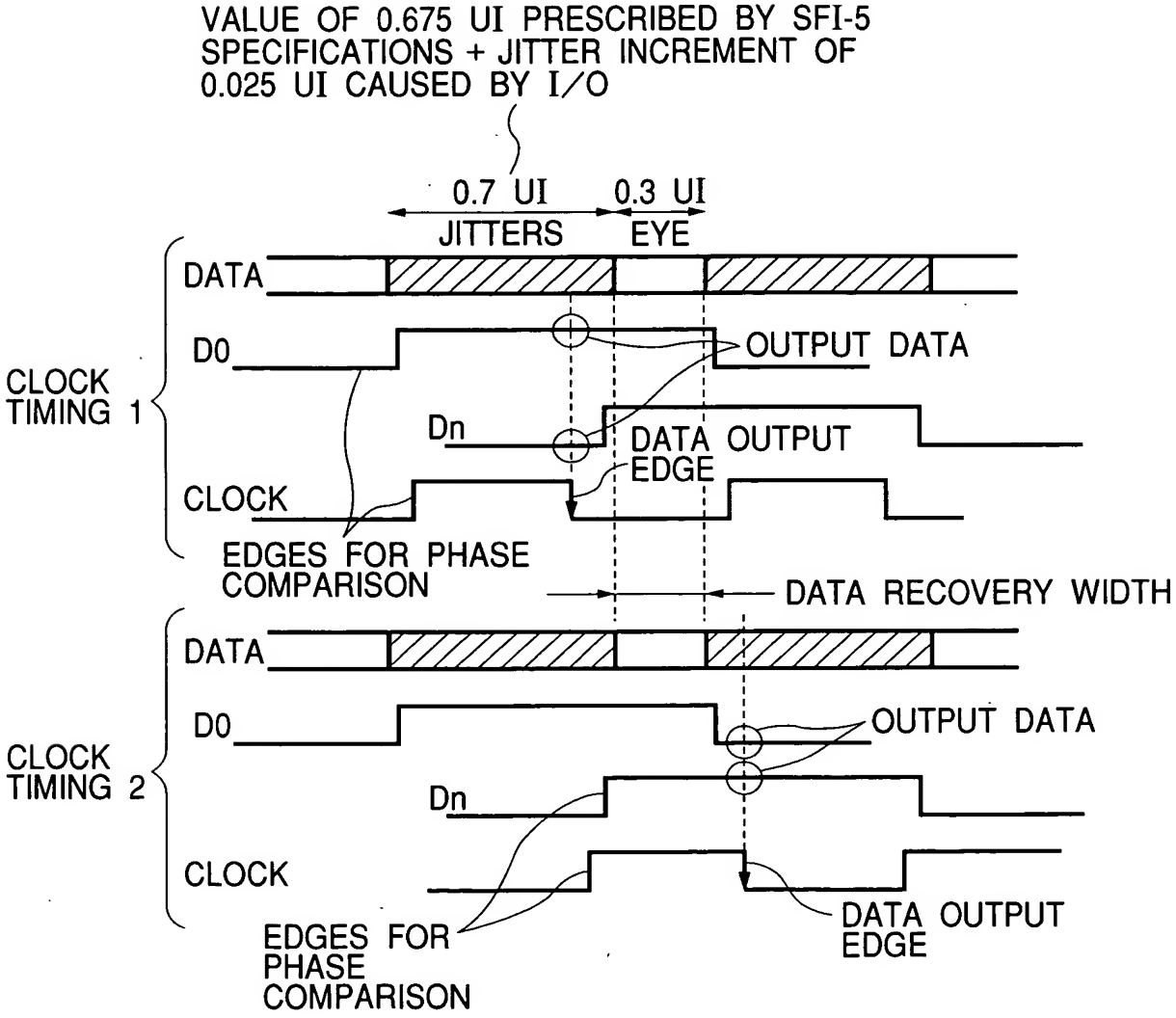
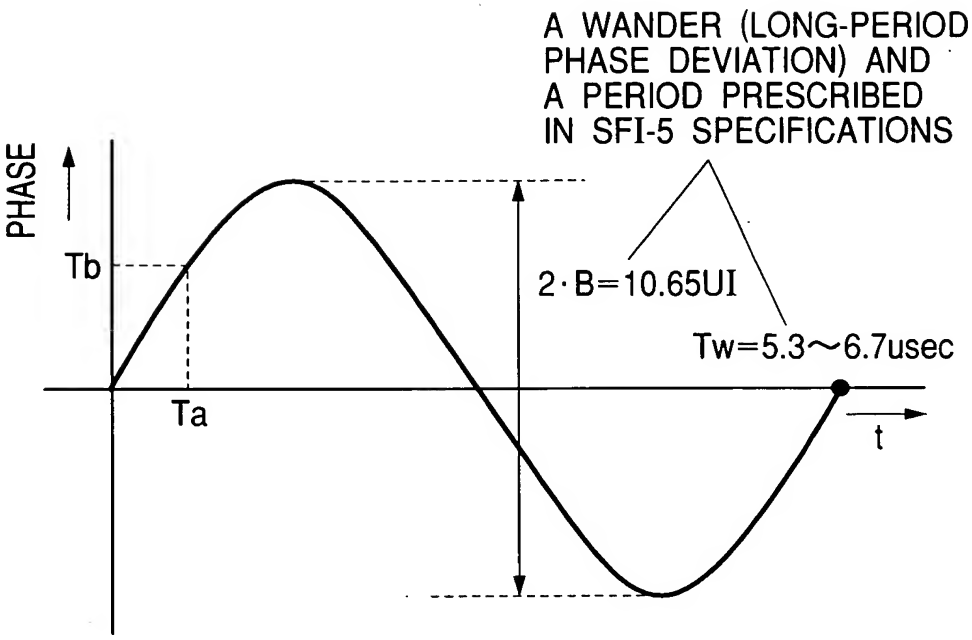

VALUE OF 0.675 UI PRESCRIBED BY SFI-5 SPECIFICATIONS + JITTER INCREMENT OF 0.025 UI CAUSED BY I/O
0.7 UI
JITTERS
0.3 UI
EYE
DATA
D0
OUTPUT DATA
CLOCK TIMING 1
Dn
DATA OUTPUT EDGE
CLOCK
EDGES FOR PHASE COMPARISON
DATA RECOVERY WIDTH
DATA
D0
OUTPUT DATA
CLOCK TIMING 2
Dn
CLOCK
DATA OUTPUT EDGE
EDGES FOR PHASE COMPARISON

FIG. 25



Ta: PHASE DETECTION PERIOD IN THE CONVENTIONAL SYSTEM, THAT IS, TIME IT TAKES TO REACH A COUNT OF N
LOOP DELAY IN THE PRESENT INVENTION, THAT IS, A PERIOD BETWEEN REFLECTION OF A PHASE COMPARISON RESULT AND PHASE COMPARISON

Tb: WANDER FOR PERIOD Ta

FIG. 26

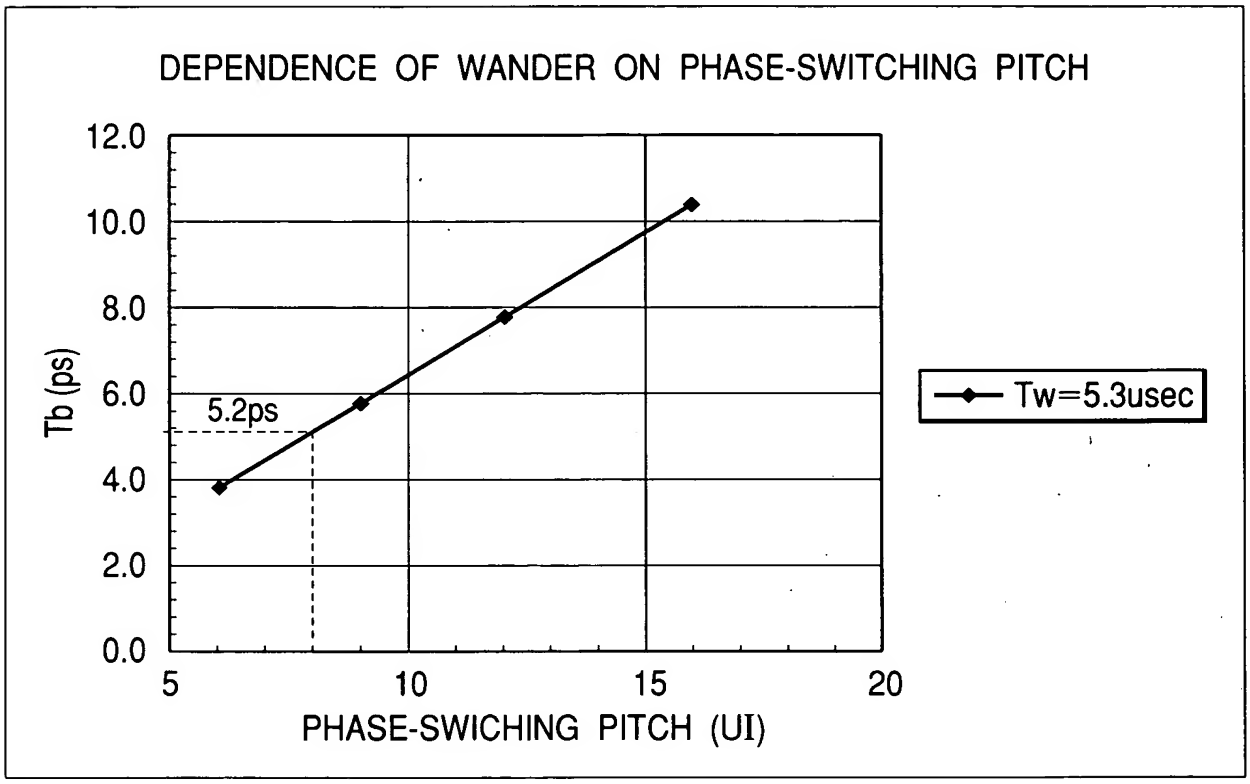

DEPENDENCE OF WANDER ON PHASE-SWITCHING PITCH
12.0
10.0
8.0
6.0
4.0
2.0
0.0
Tb (ps)
5.2ps
5
10
15
20
PHASE-SWICHING PITCH (UI)
Tw=5.3usec

FIG. 27

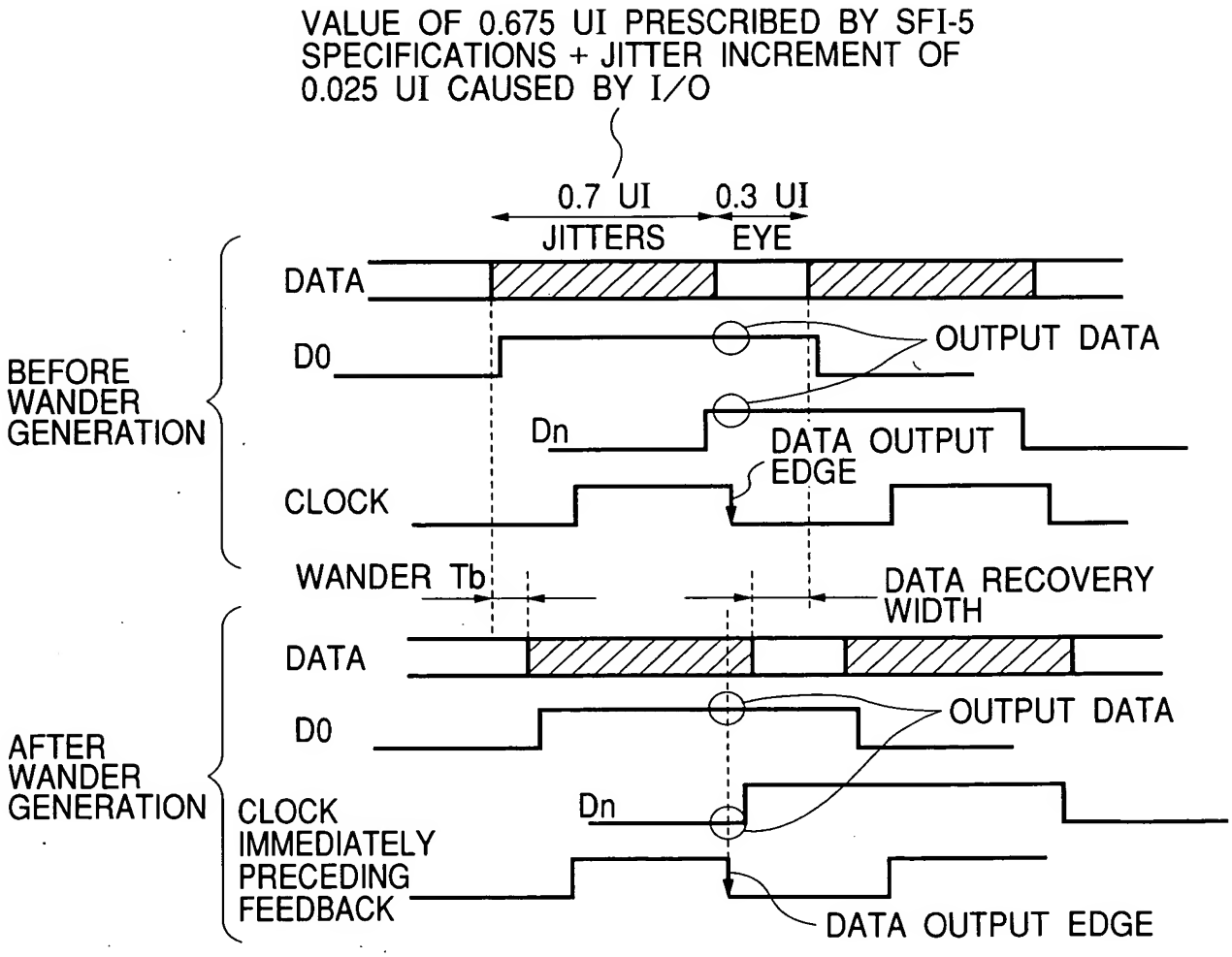
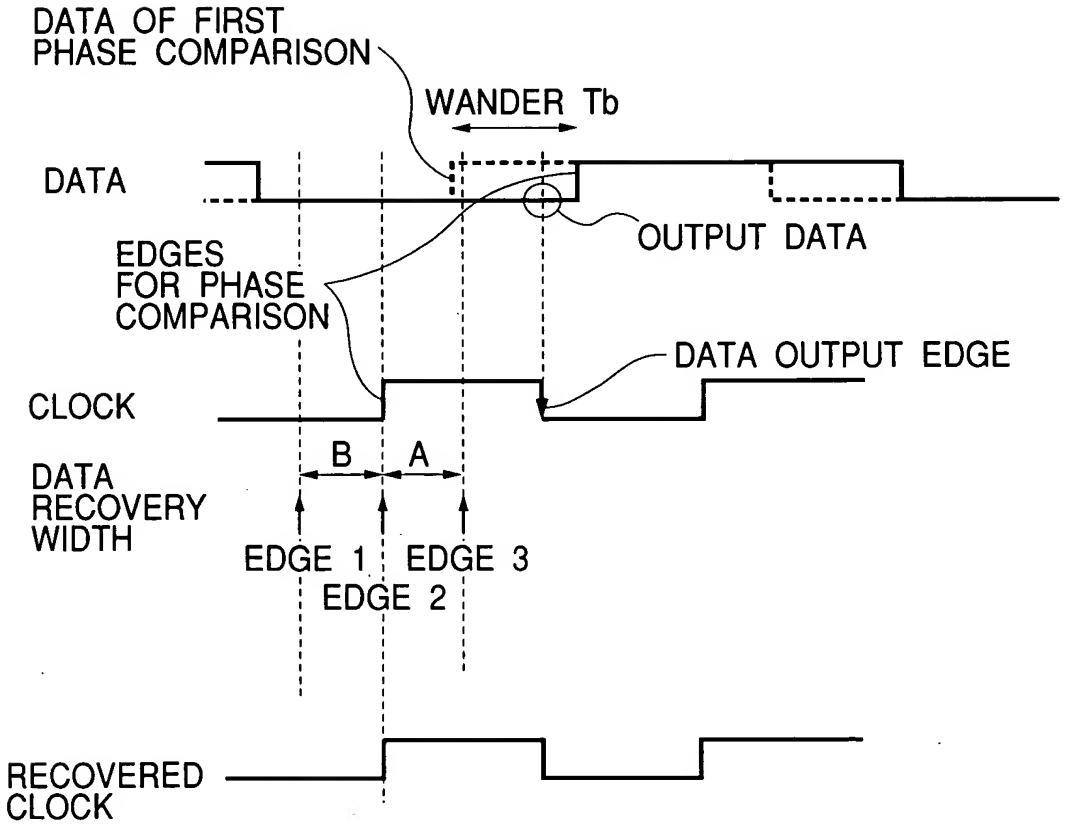

VALUE OF 0.675 UI PRESCRIBED BY SFI-5 SPECIFICATIONS + JITTER INCREMENT OF 0.025 UI CAUSED BY I/O
0.7 UI
JITTERS
0.3 UI
EYE
DATA
D0
OUTPUT DATA
Dn
DATA OUTPUT EDGE
CLOCK
BEFORE WANDER GENERATION
WANDER Tb
DATA RECOVERY WIDTH
DATA
D0
OUTPUT DATA
Dn
CLOCK IMMEDIATELY PRECEDING FEEDBACK
AFTER WANDER GENERATION
DATA OUTPUT EDGE

FIG. 28


DATA OF FIRST
PHASE COMPARISON
WANDER Tb
DATA
OUTPUT DATA
EDGES
FOR PHASE
COMPARISON
DATA OUTPUT EDGE
CLOCK
B
A
DATA
RECOVERY
WIDTH
EDGE 1
EDGE 3
EDGE 2
RECOVERED
CLOCK